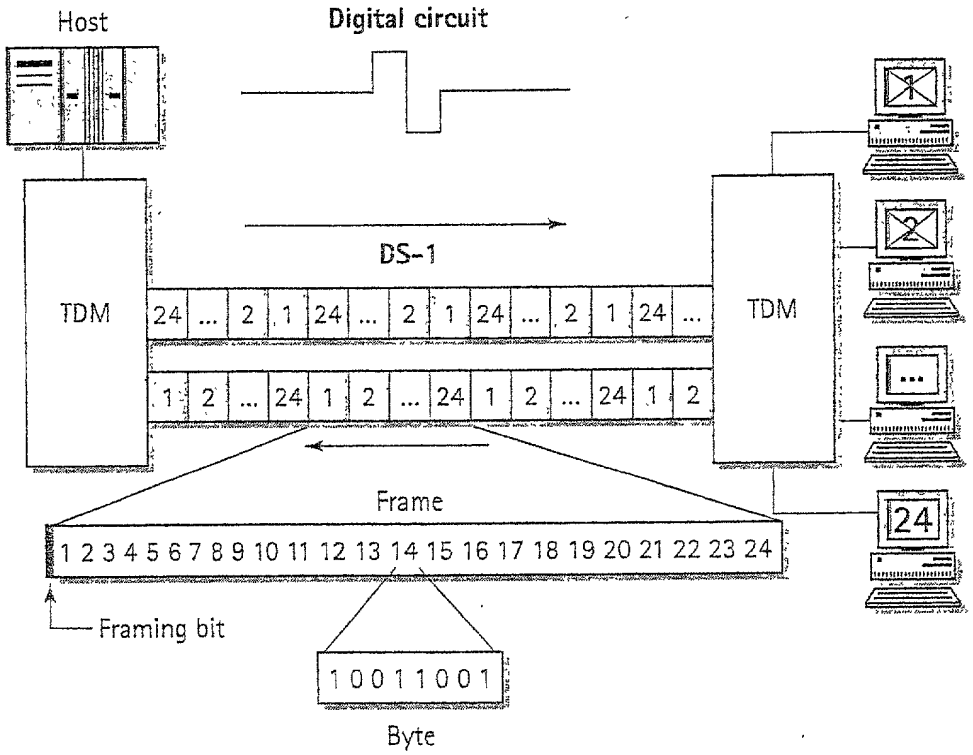

Host
Digital circuit
TDM
DS-1
TDM
24 ... 2 1 24 ... 2 1 24 ... 2 1 24 ...
1 2 ... 24 1 2 ... 24 1 2 ... 24 1 2
Frame
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Framing bit
10011001
Byte
24

Figure 1

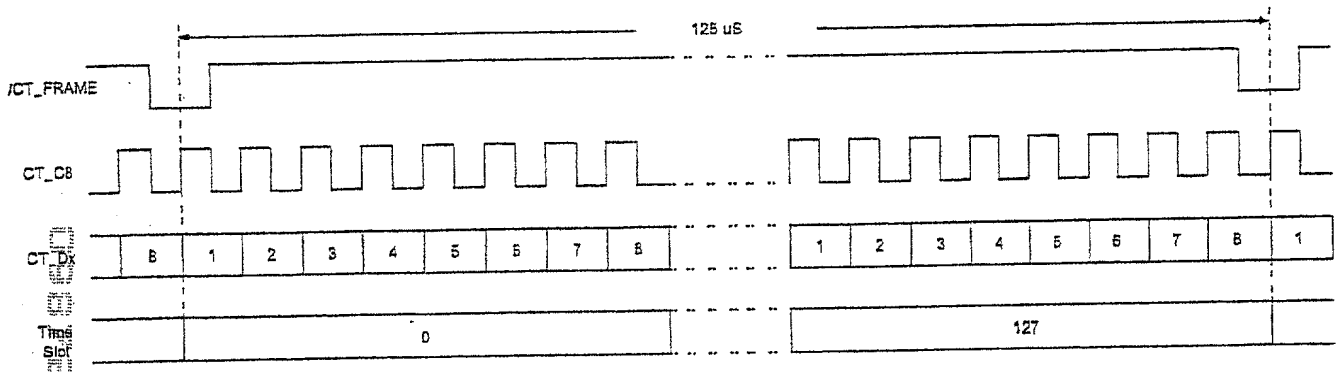

125 uS
/CT_FRAME
CT_C8
CT_Dx
B
1
2
3
4
5
6
7
8
1
2
3
4
5
6
7
8
1
Time Slot
0
127

Figure 2

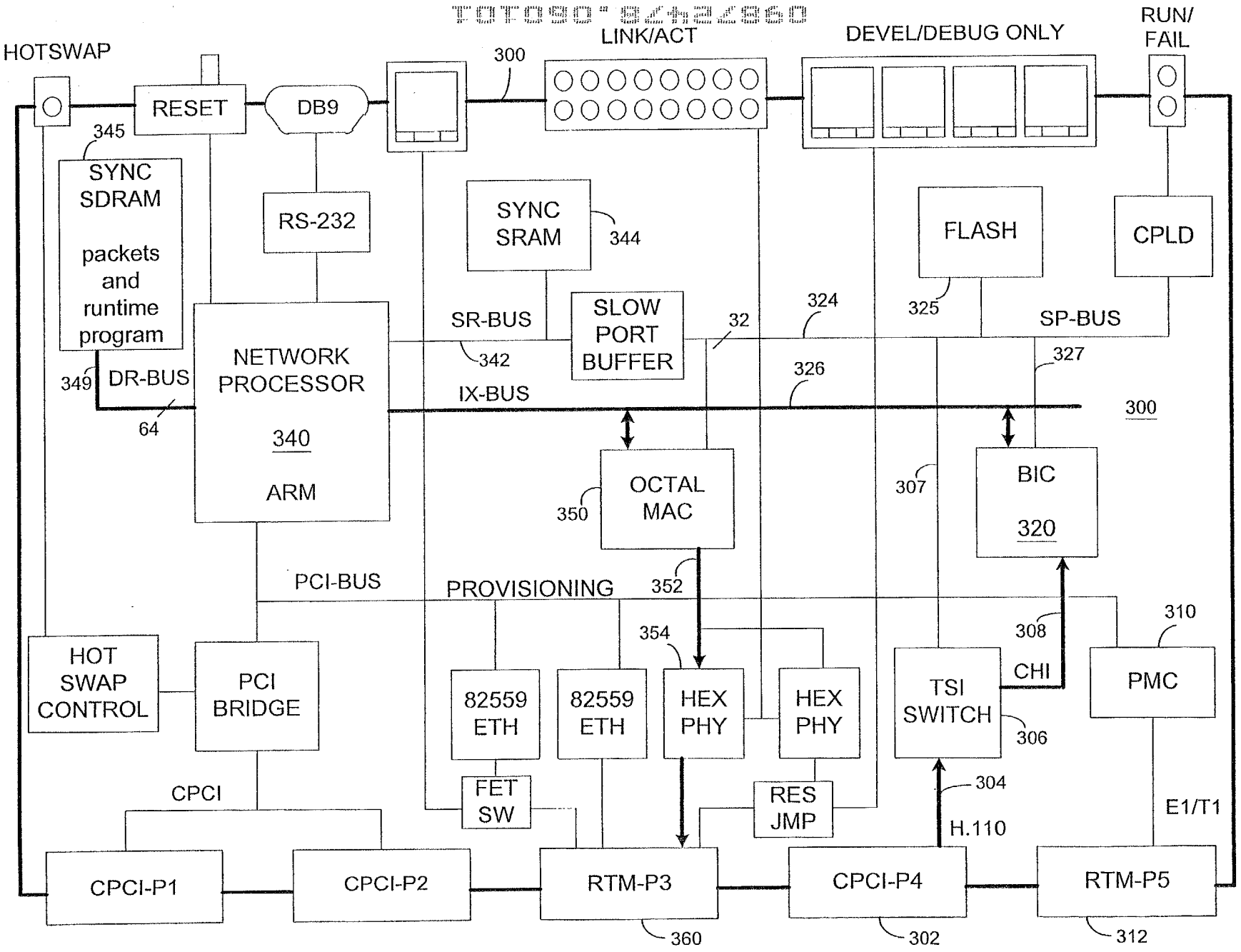

HOTSWAP
RESET
DB9
300
LINK/ACT
DEVEL/DEBUG ONLY
RUN/
FAIL
345
SYNC
SDRAM
packets
and
runtime
program
RS-232
SYNC
SRAM
344
FLASH
CPLD
325
SR-BUS
342
SLOW
PORT
BUFFER
32
324
SP-BUS
327
349
DR-BUS
64
NETWORK
PROCESSOR
340
ARM
IX-BUS
326
300
OCTAL
MAC
350
307
BIC
320
PCI-BUS
PROVISIONING
352
354
308
310
HOT
SWAP
CONTROL
PCI
BRIDGE
82559
ETH
82559
ETH
HEX
PHY
HEX
PHY
TSI
SWITCH
CHI
306
PMC
CPCI
FET
SW
RES
JMP
304
H.110
E1/T1
CPCI-P1
CPCI-P2
RTM-P3
CPCI-P4
RTM-P5
360
302
312

Figure 3

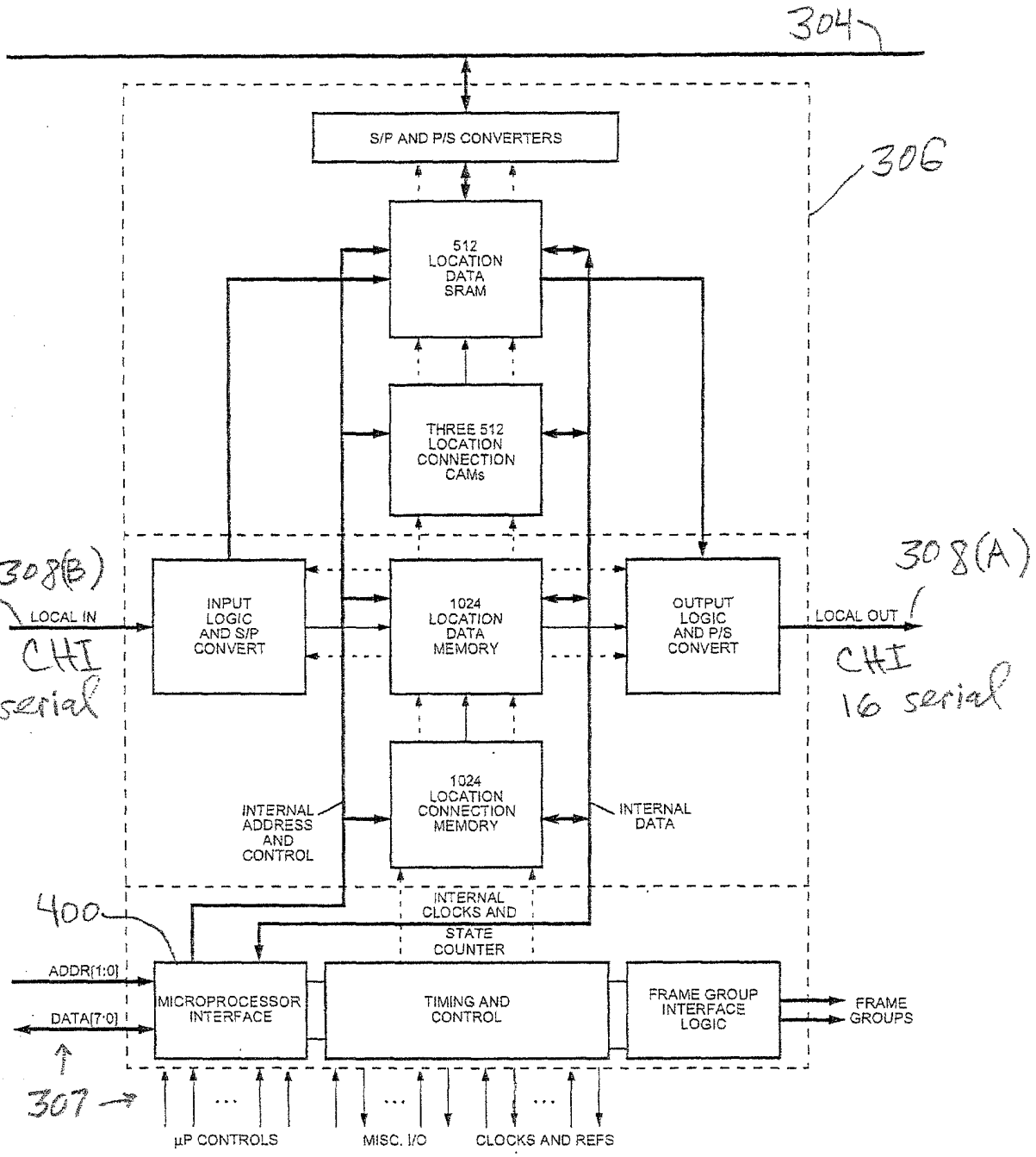

304
S/P AND P/S CONVERTERS
306
512 LOCATION DATA SRAM
THREE 512 LOCATION CONNECTION CAMs
308(B)
LOCAL IN
CHI 16 serial
INPUT LOGIC AND S/P CONVERT
1024 LOCATION DATA MEMORY
OUTPUT LOGIC AND P/S CONVERT
308(A)
LOCAL OUT
CHI 16 serial
1024 LOCATION CONNECTION MEMORY
INTERNAL ADDRESS AND CONTROL
INTERNAL DATA
400
INTERNAL CLOCKS AND STATE COUNTER
ADDR[1:0]
DATA[7:0]
MICROPROCESSOR INTERFACE
TIMING AND CONTROL
FRAME GROUP INTERFACE LOGIC
FRAME GROUPS
307
µP CONTROLS
MISC. I/O
CLOCKS AND REFS

Figure 4

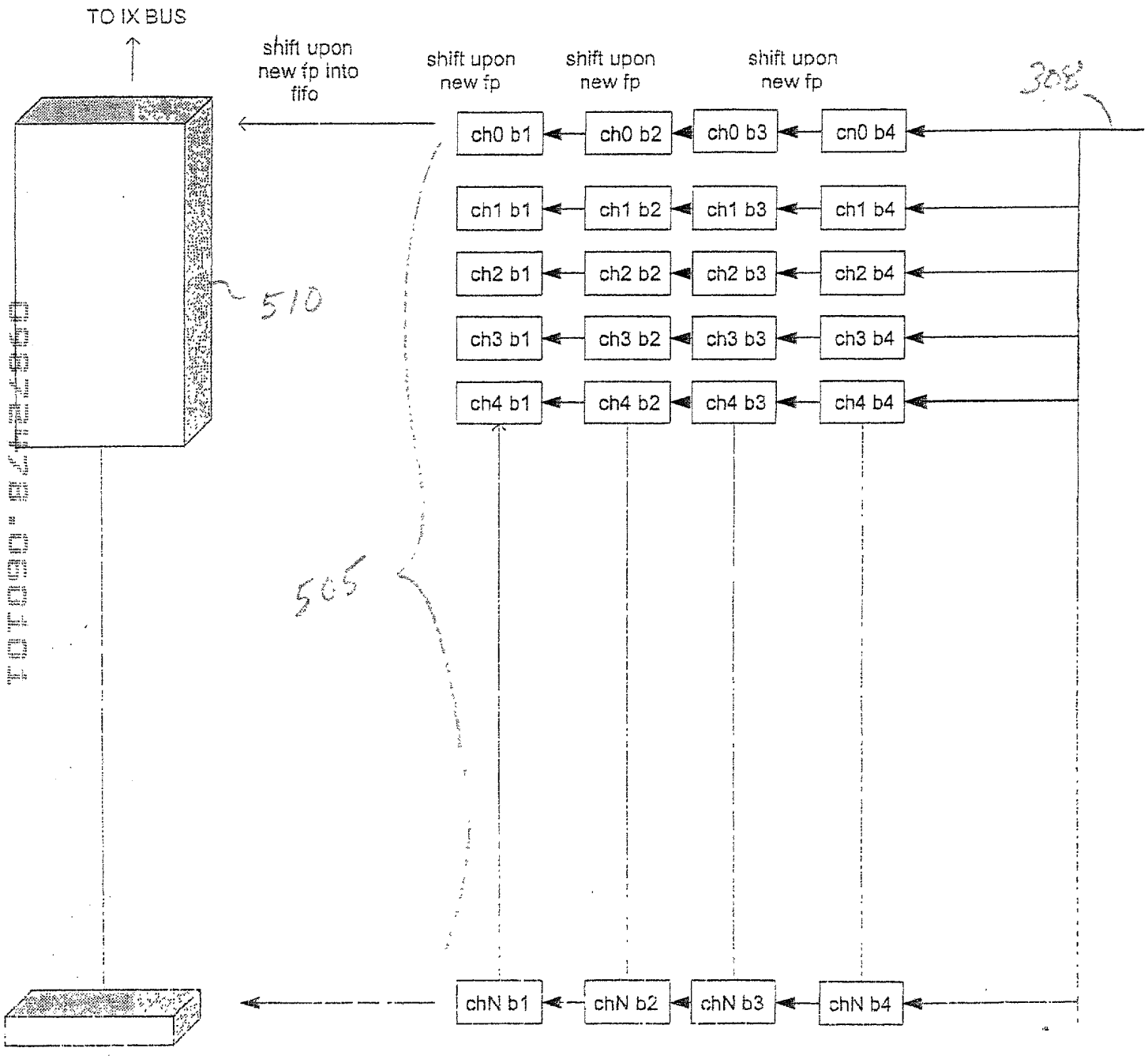

TO IX BUS
shift upon new fp into fifo
shift upon new fp
shift upon new fp
shift upon new fp
ch0 b1
ch0 b2
ch0 b3
cn0 b4
ch1 b1
ch1 b2
ch1 b3
ch1 b4
ch2 b1
ch2 b2
ch2 b3
ch2 b4
ch3 b1
ch3 b2
ch3 b3
ch3 b4
ch4 b1
ch4 b2
ch4 b3
ch4 b4
chN b1
chN b2
chN b3
chN b4
510
505
308

Figure 5

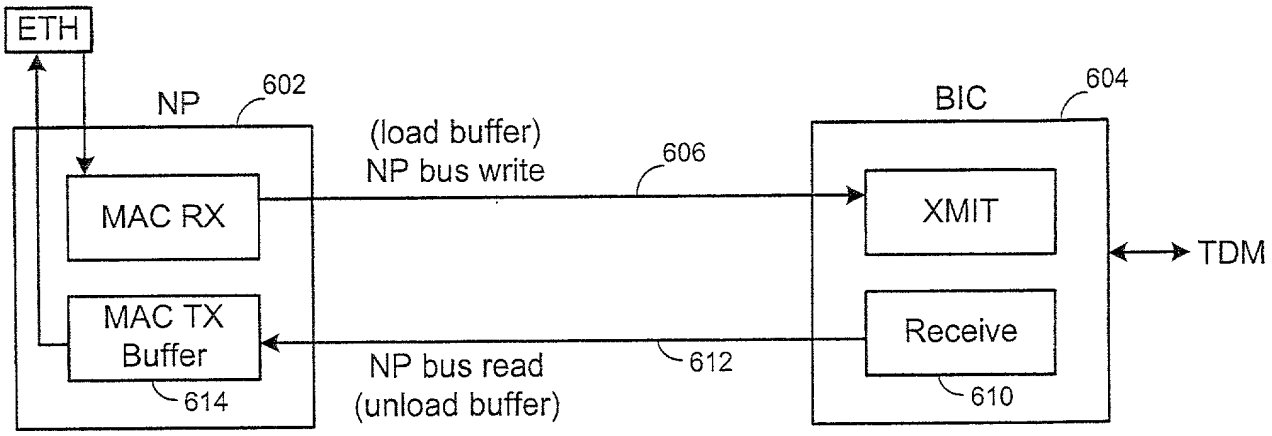


Figure 6A

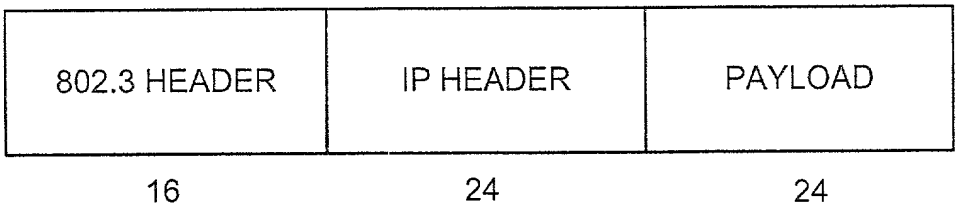


Figure 6B

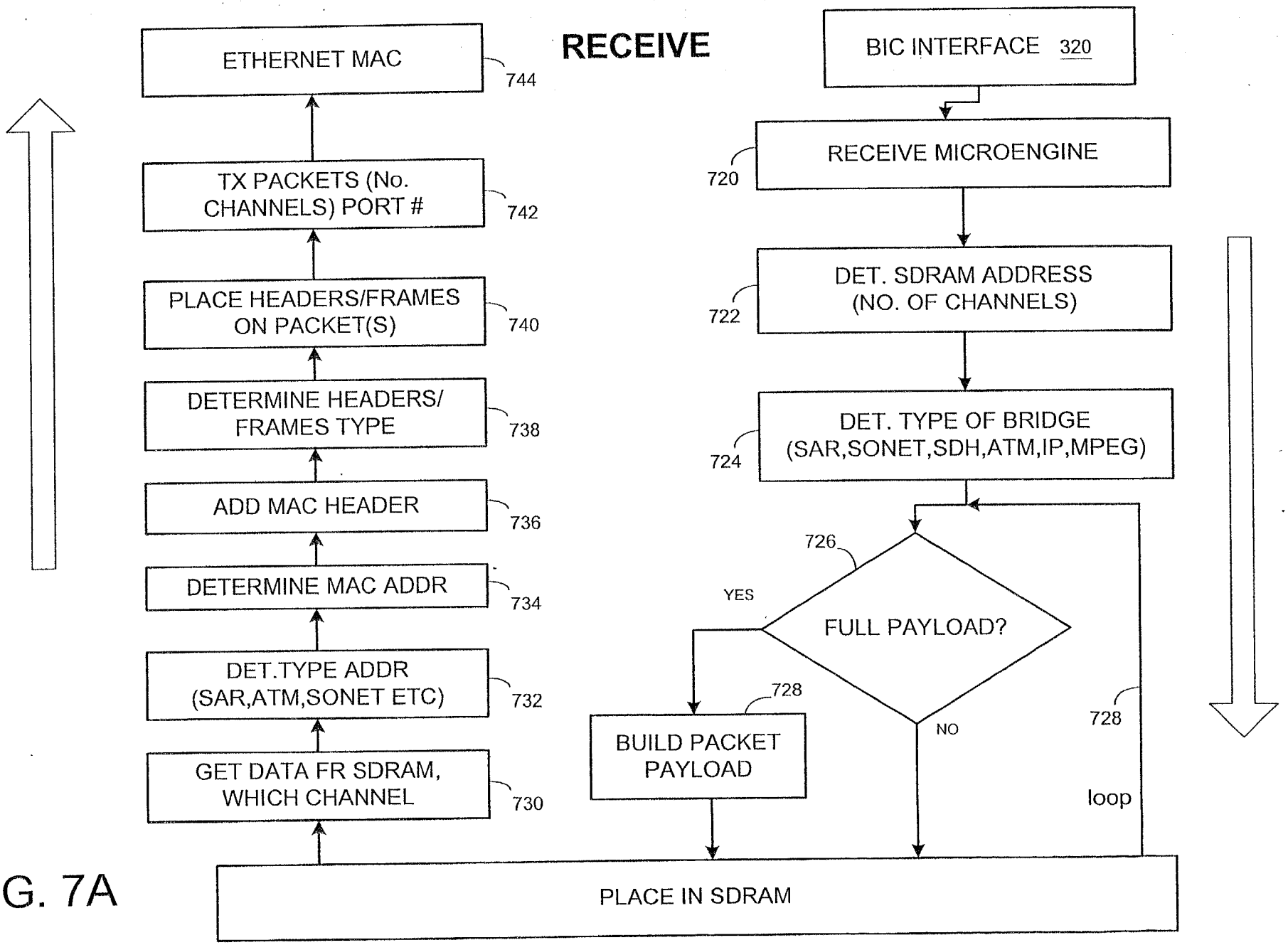

RECEIVE
BIC INTERFACE 320
RECEIVE MICROENGINE
720
DET. SDRAM ADDRESS (NO. OF CHANNELS)
722
DET. TYPE OF BRIDGE (SAR,SONET,SDH,ATM,IP,MPEG)
724
726
FULL PAYLOAD?
YES
NO
728
BUILD PACKET PAYLOAD
728
loop
PLACE IN SDRAM
ETHERNET MAC
744
TX PACKETS (No. CHANNELS) PORT #
742
PLACE HEADERS/FRAMES ON PACKET(S)
740
DETERMINE HEADERS/ FRAMES TYPE
738
ADD MAC HEADER
736
DETERMINE MAC ADDR
734
DET.TYPE ADDR (SAR,ATM,SONET ETC)
732
GET DATA FR SDRAM, WHICH CHANNEL
730

FIG. 7A

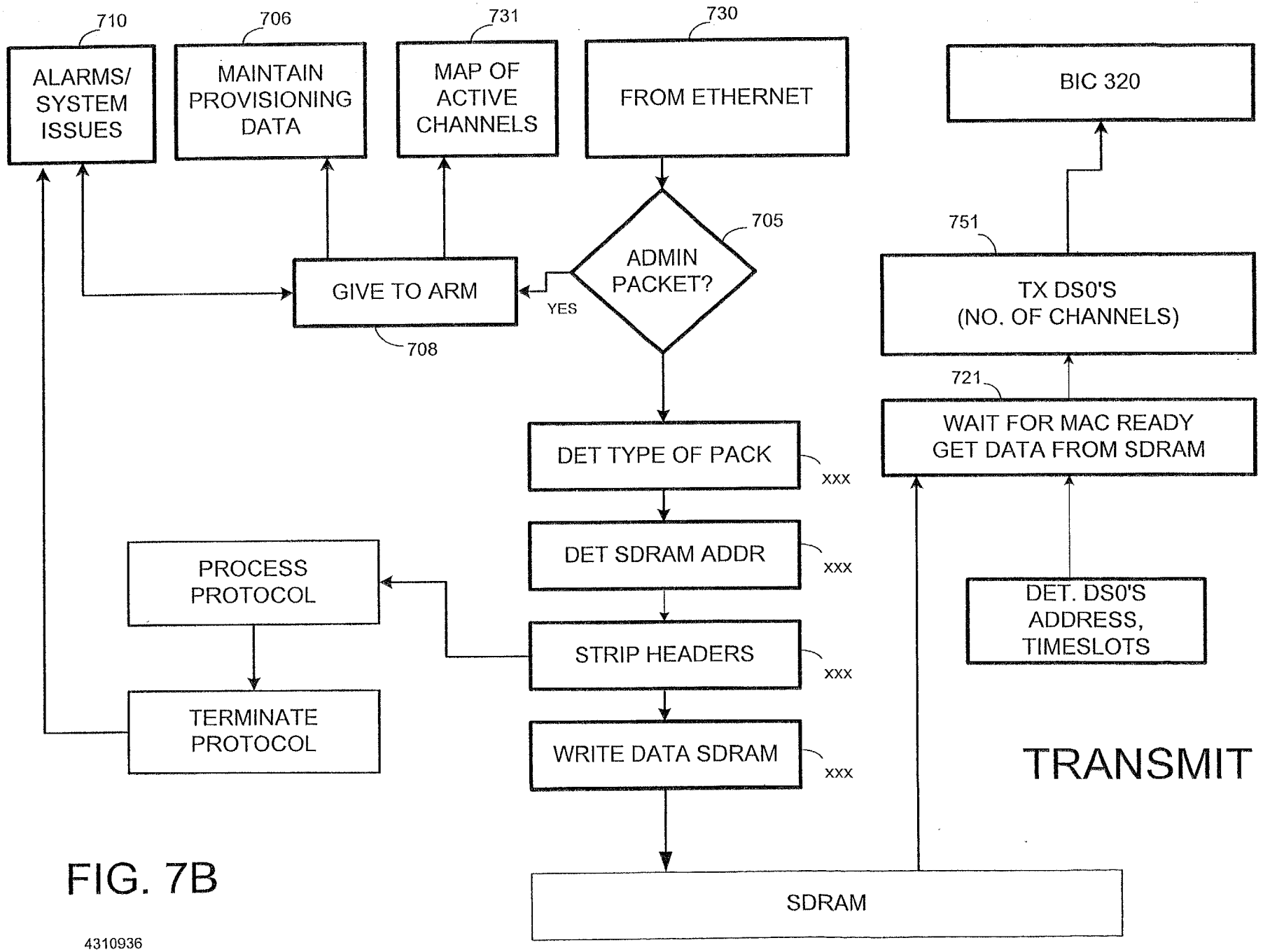

710
ALARMS/ SYSTEM ISSUES
706
MAINTAIN PROVISIONING DATA
731
MAP OF ACTIVE CHANNELS
730
FROM ETHERNET
BIC 320
705
ADMIN PACKET?
YES
GIVE TO ARM
708
751
TX DS0'S (NO. OF CHANNELS)
721
WAIT FOR MAC READY GET DATA FROM SDRAM
DET TYPE OF PACK
xxx
DET SDRAM ADDR
xxx
PROCESS PROTOCOL
STRIP HEADERS
xxx
DET. DS0'S ADDRESS, TIMESLOTS
TERMINATE PROTOCOL
WRITE DATA SDRAM
xxx
TRANSMIT
SDRAM

FIG. 7B

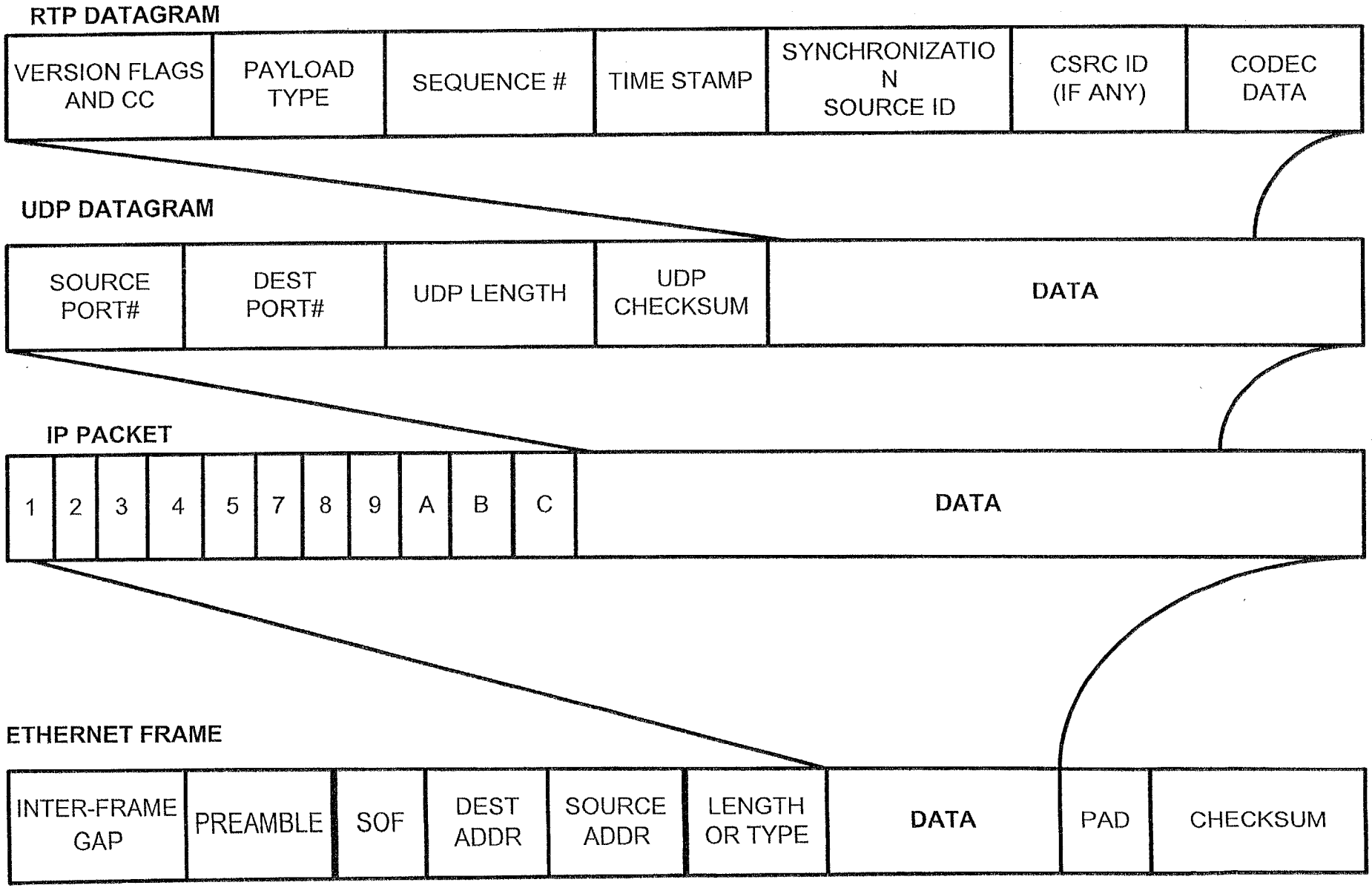


Figure 8

4303606

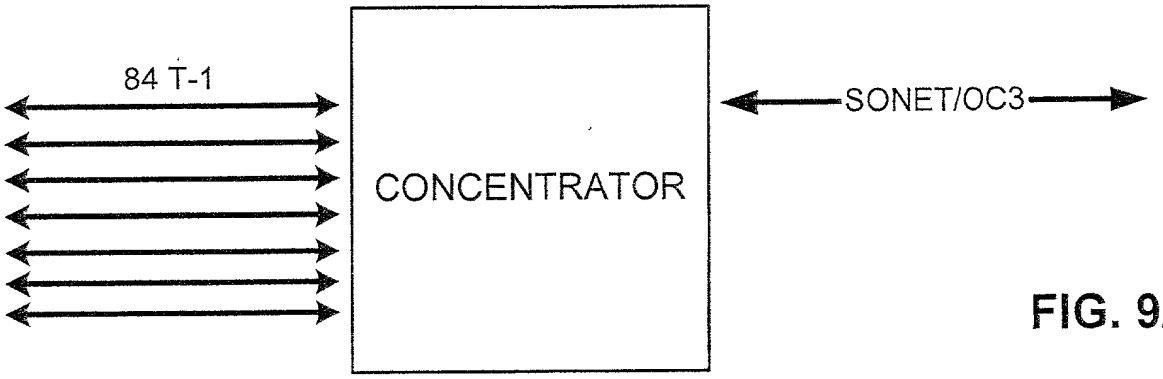


FIG. 9A

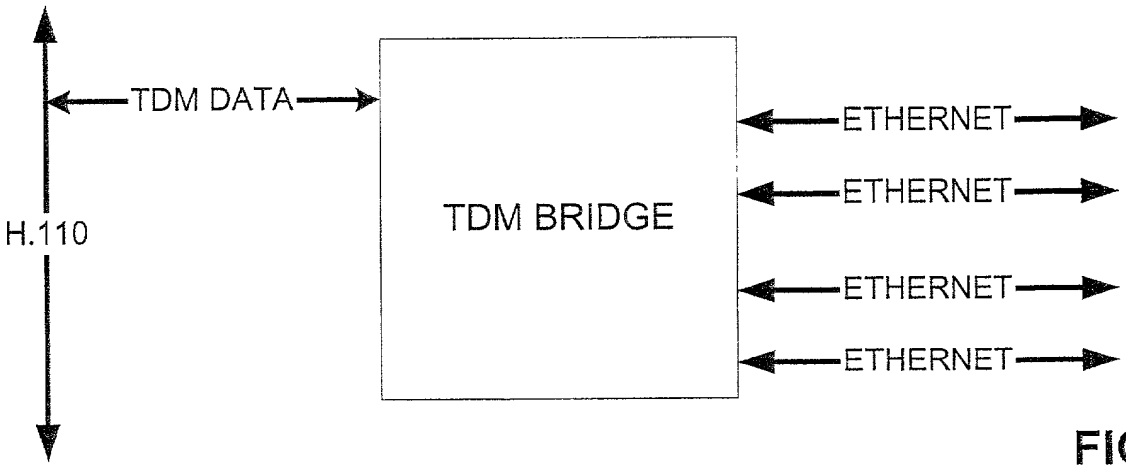


FIG. 9B

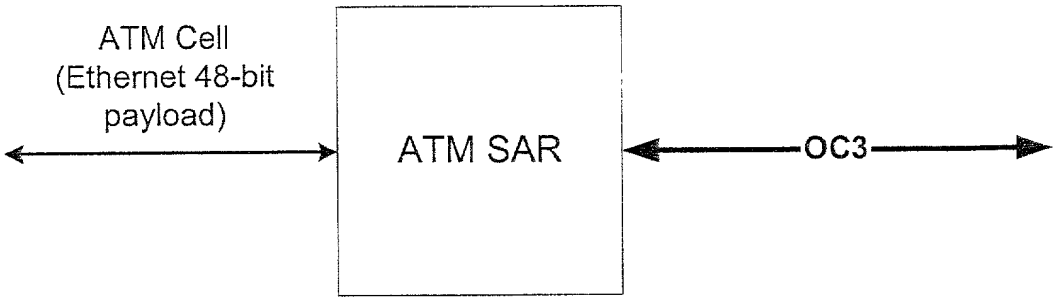


FIG. 10A

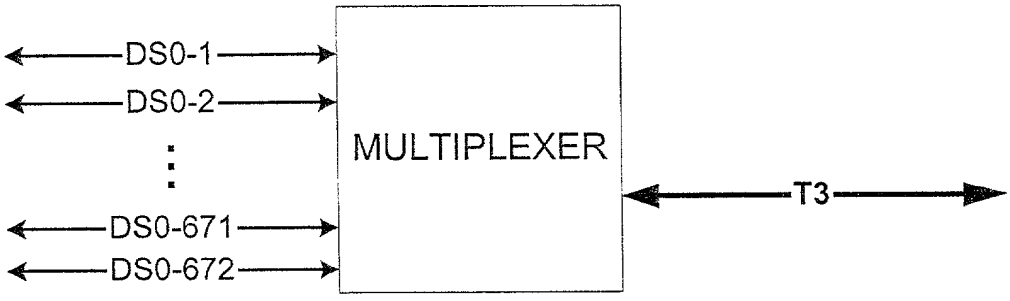


FIG. 10B

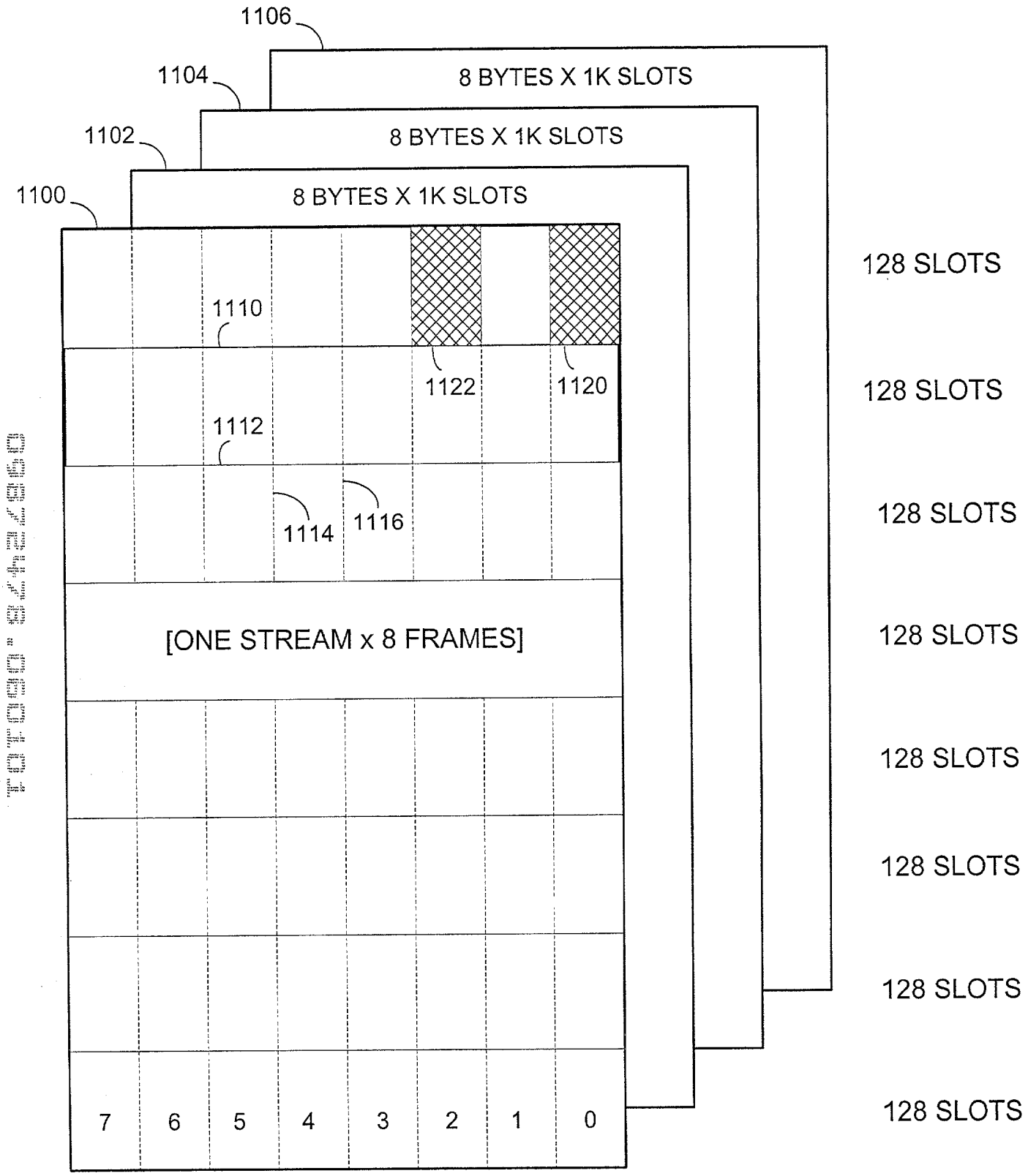

1106
1104
1102
1100
8 BYTES X 1K SLOTS
8 BYTES X 1K SLOTS
8 BYTES X 1K SLOTS
1110
1122
1120
1112
1114
1116
[ONE STREAM x 8 FRAMES]
7
6
5
4
3
2
1
0
128 SLOTS
128 SLOTS
128 SLOTS
128 SLOTS
128 SLOTS
128 SLOTS
128 SLOTS
128 SLOTS

Figure 11

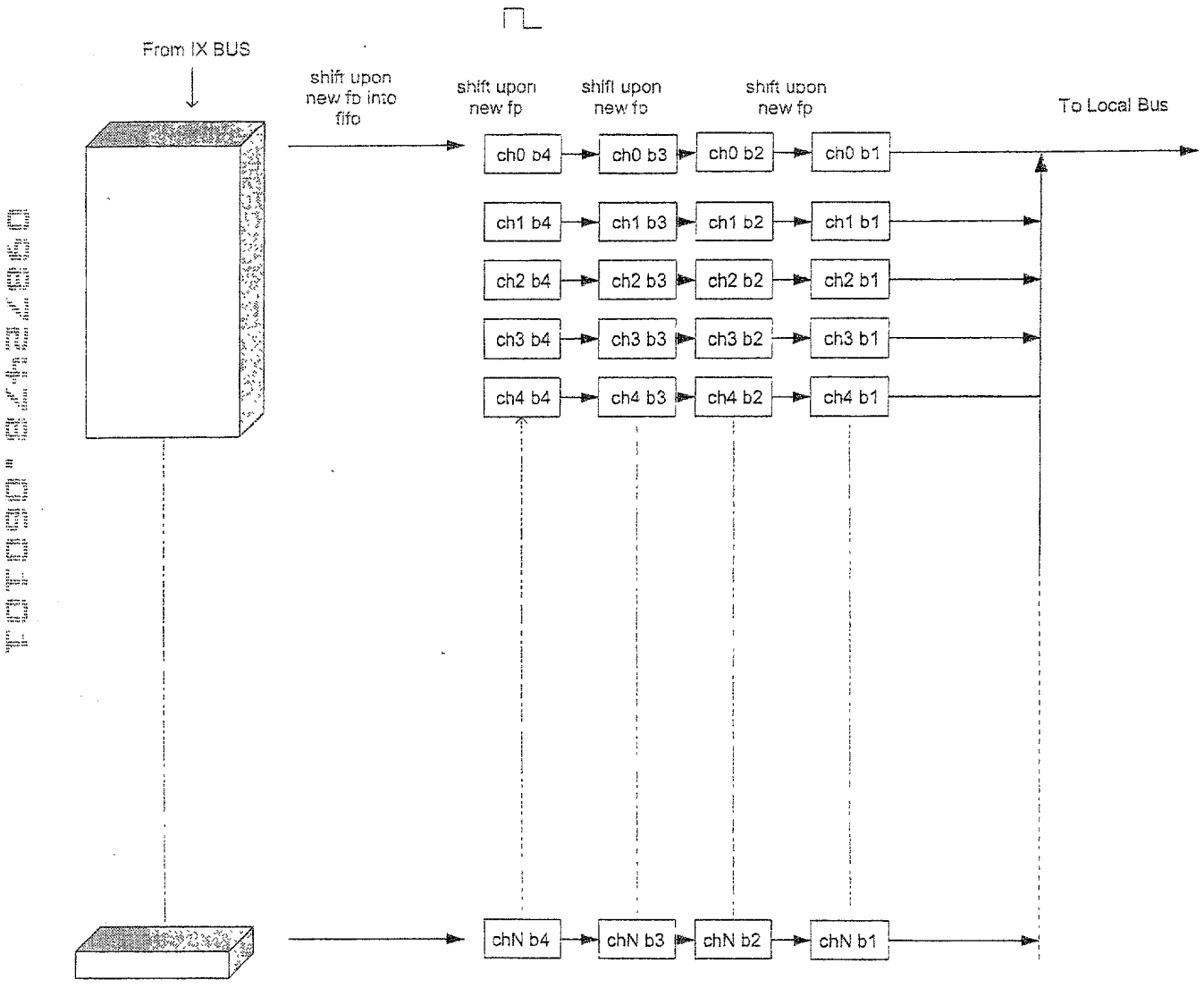

From IX BUS
shift upon new fp into fifo
shift upon new fp
shift upon new fp
shift upon new fp
To Local Bus
ch0 b4
ch0 b3
ch0 b2
ch0 b1
ch1 b4
ch1 b3
ch1 b2
ch1 b1
ch2 b4
ch2 b3
ch2 b2
ch2 b1
ch3 b4
ch3 b3
ch3 b2
ch3 b1
ch4 b4
ch4 b3
ch4 b2
ch4 b1
chN b4
chN b3
chN b2
chN b1

Figure 12

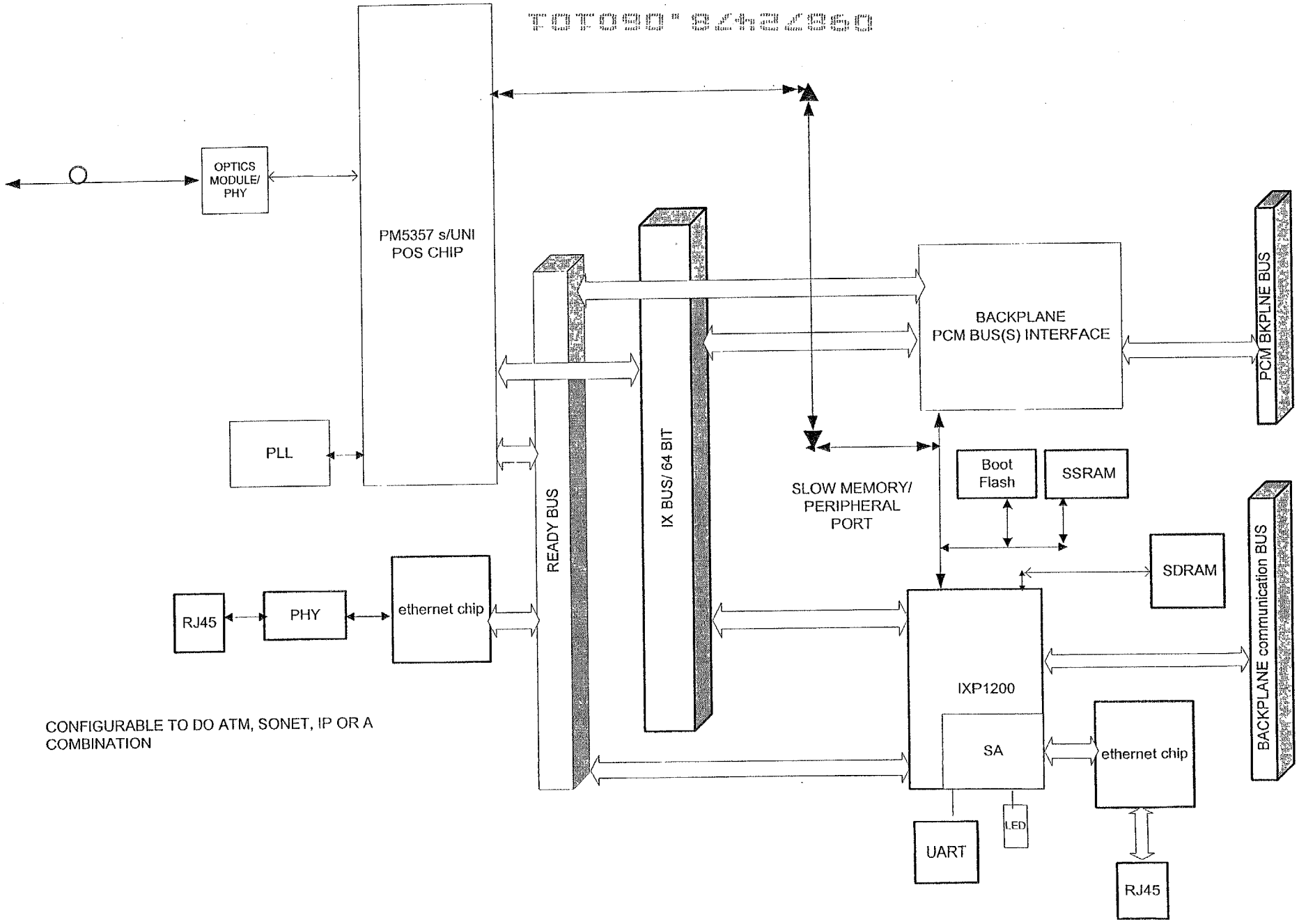


Figure 13

4307665

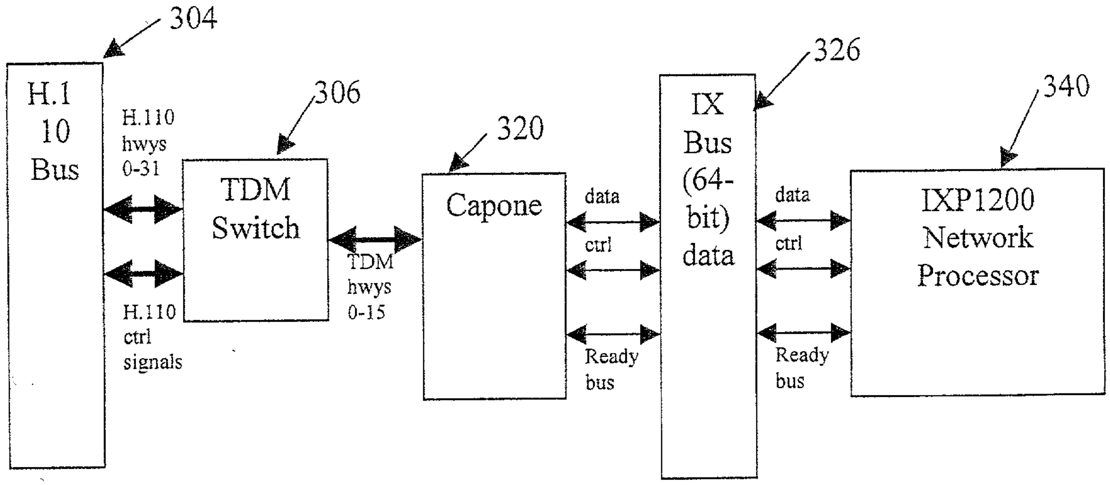

304
H.1
10
Bus
H.110
hwys
0-31
H.110
ctrl
signals
306
TDM
Switch
TDM
hwys
0-15
320
Capone
data
ctrl
Ready
bus
326
IX
Bus
(64-
bit)
data
data
ctrl
Ready
bus
340
IXP1200
Network
Processor

Figure 15

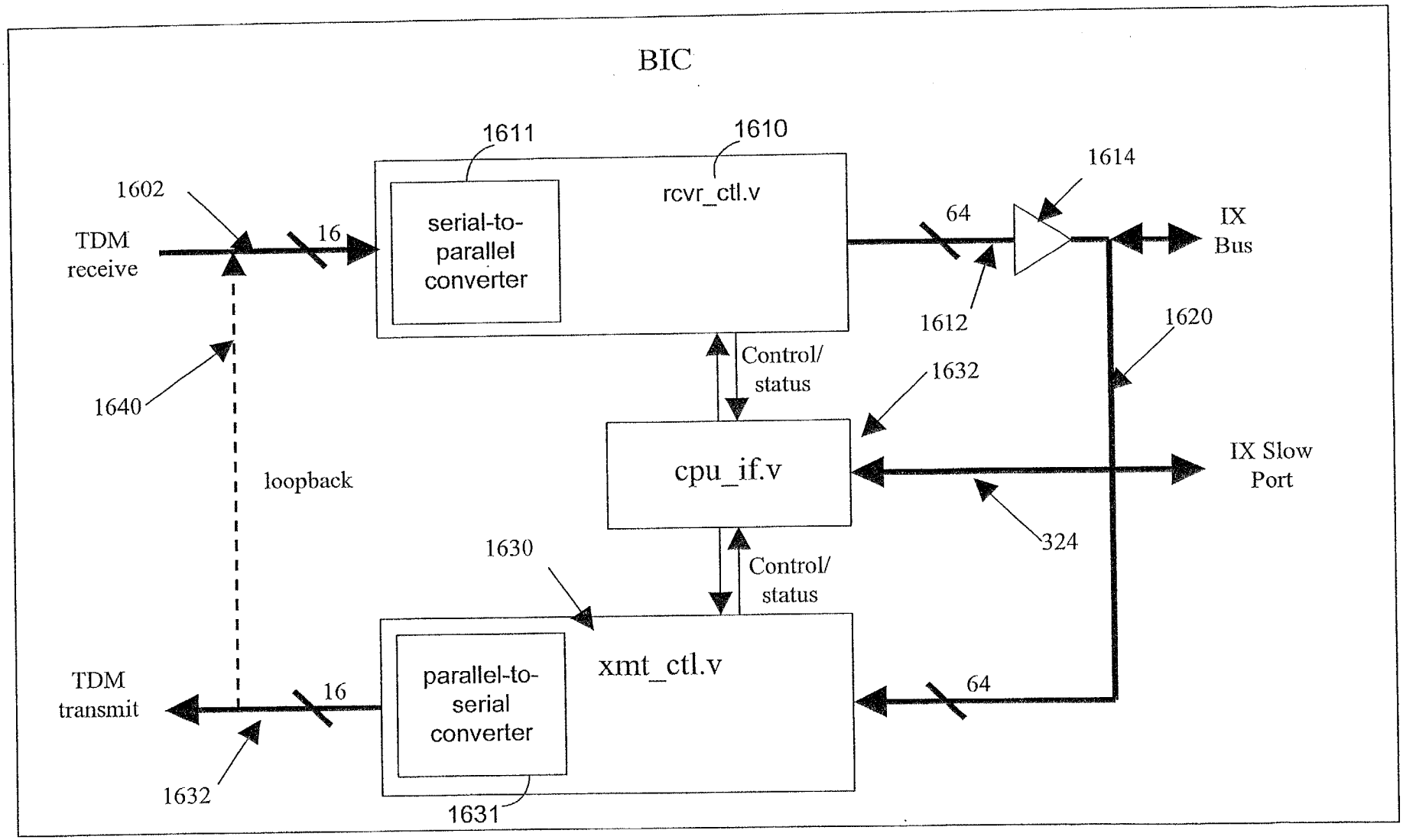
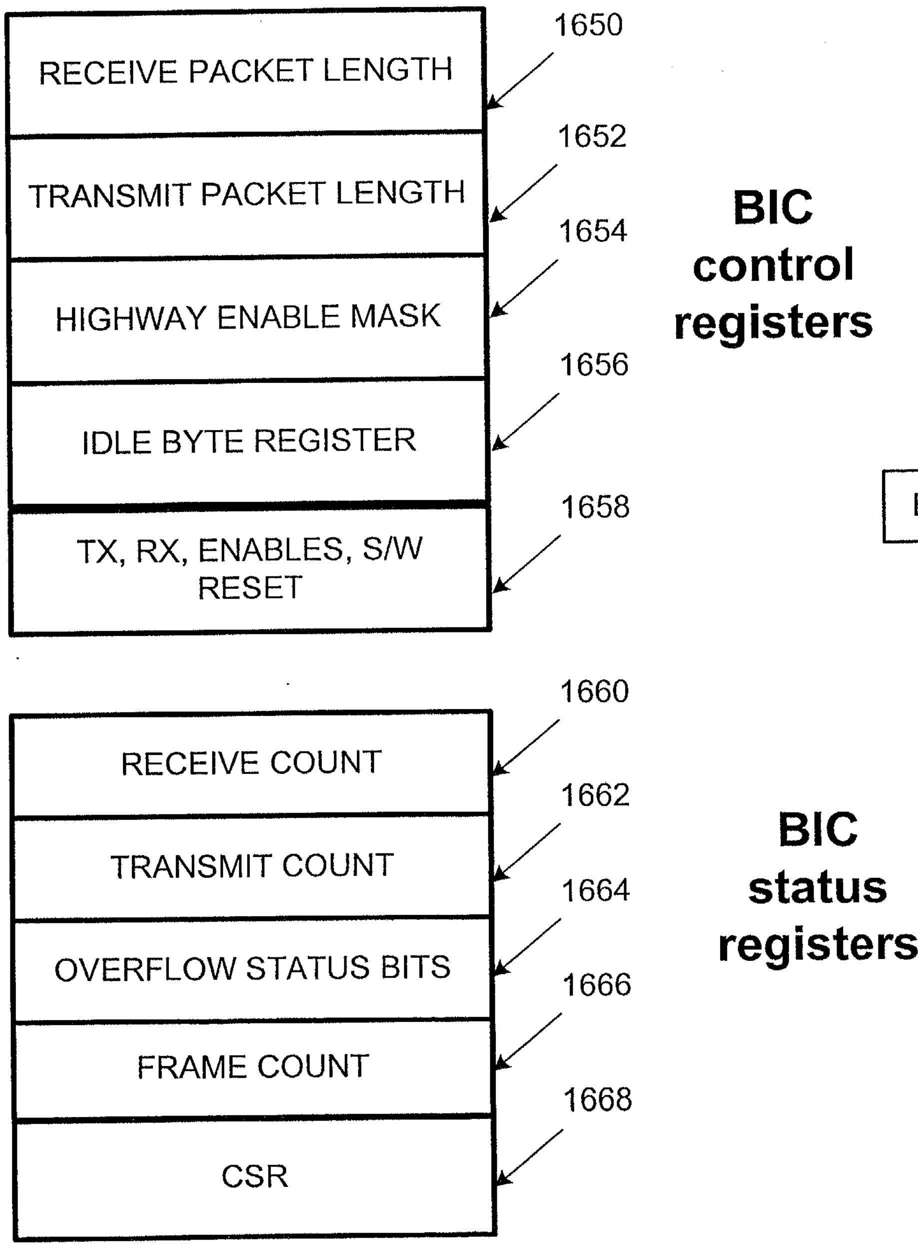

BIC
1611
1610
1614
1602
rcvr_ctl.v
TDM
receive
16
serial-to-
parallel
converter
64
IX
Bus
1612
1620
Control/
status
1632
1640
cpu_if.v
IX Slow
Port
loopback
324
1630
Control/
status
xmt_ctl.v
TDM
transmit
16
parallel-to-
serial
converter
64
1632
1631

Figure 16A



4303606

Figure 16B

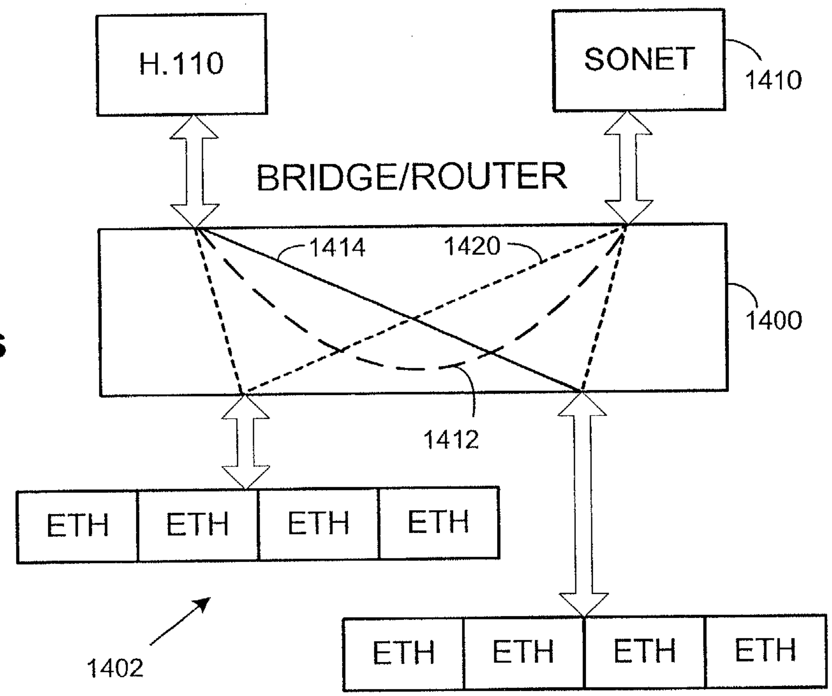


Figure 14

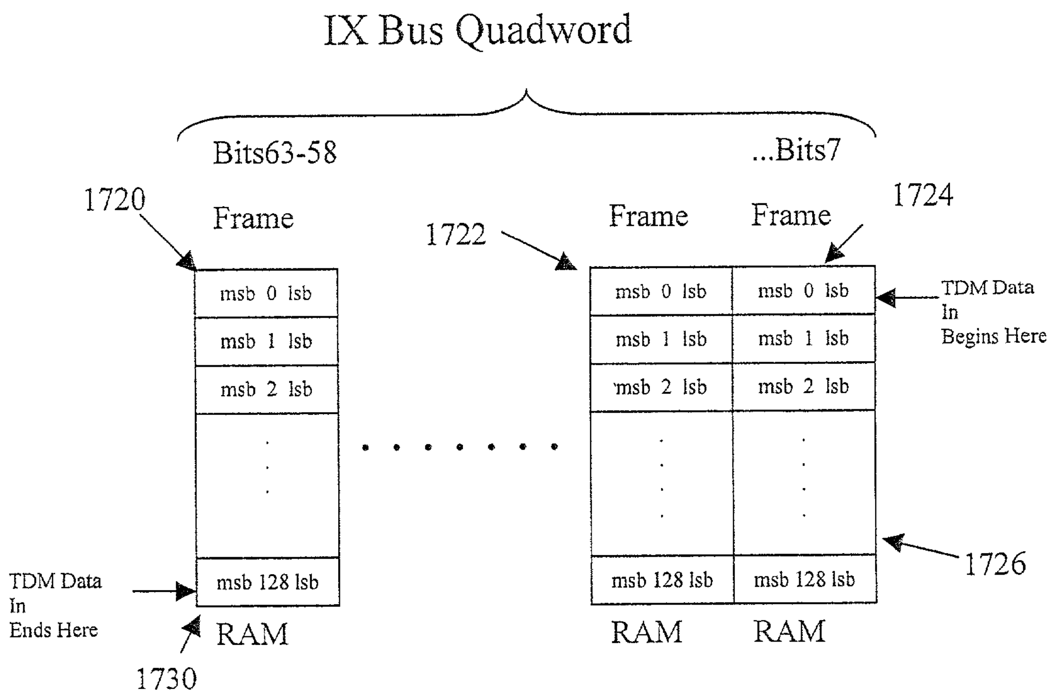

IX Bus Quadword
Bits63-58
...Bits7
1720
Frame
1722
Frame
Frame
1724
msb 0 lsb
msb 1 lsb
msb 2 lsb
msb 128 lsb
TDM Data In Begins Here
TDM Data In Ends Here
1726
1730
RAM
RAM
RAM

Figure 17

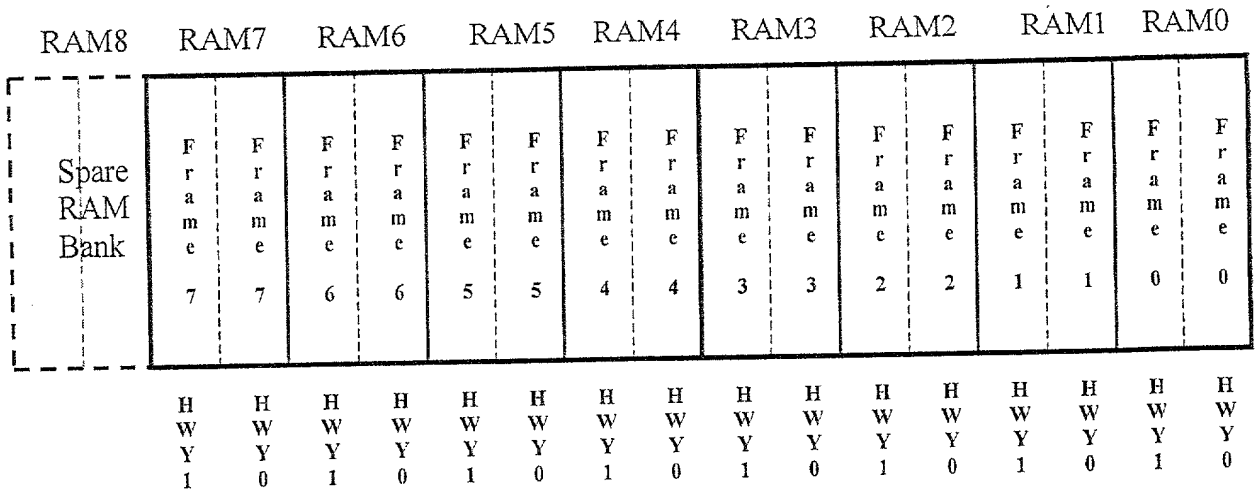


Figure 18

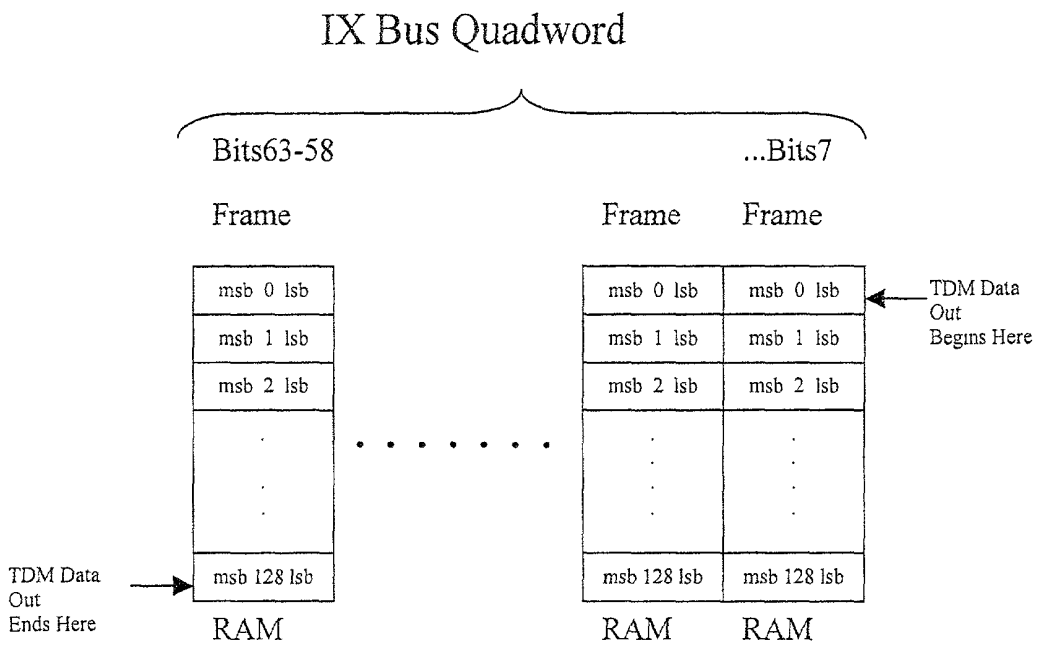


Figure 19

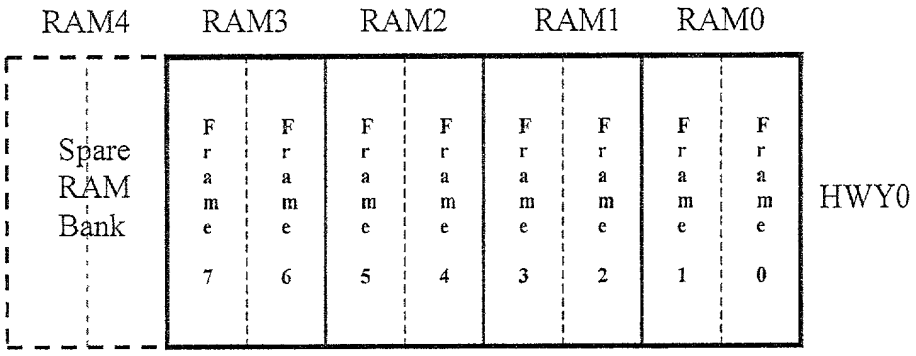


Figure 20